AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [00116] with the following amended paragraph:

[0116] Programming circuitry 1400 includes a variable bit line load 1420 and a variable source line bias circuit 1450. Variable bit line load 1420 is connected to multi-level verify/read circuits 1440. Signals PGM, Source Bias Disable, ~~VFY+Read~~ VFY+Read and VFY+Read+Source Bias Disable control variable source line bias circuit 1450. A full 4-BPC memory would further include at least X similar variable bit line load and source line bias circuits, where X is the number of memory cells simultaneously accessed during a write operation. For memory cell 1410, I/O lines 1435 and a column select device 1430, which is under control of a signal Column Select N, connect variable bit line load 1420 to bit line 1416 when a write operation selects memory cell 1410. The source line 1418 of memory cell 1410 is connected to source line bias circuit 1450.